

2026 IEEE 27th Latin American Test Symposium (LATS 2026)

**Florianópolis, Brazil
17-20 March 2026**

IEEE Catalog Number:
ISBN:

CFP26LAT-POD
979-8-3195-4236-6



Copyright © 2026, IEEE

All Rights Reserved

Copyright and Reprint Permissions:

Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

*** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.

IEEE Catalog Number:	CFP26LAT-POD
ISBN (Print-On-Demand):	979-8-3195-4236-6
ISBN (Online):	979-8-3195-4235-9
ISSN:	2373-0862

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA

Phone:	(845) 758-0400
Fax:	(845) 758-2633
E-mail:	curran@proceedings.com
Web:	www.proceedings.com

TABLE OF CONTENTS

Adaptive Neural Network Optimization of Vehicle Start-Stop Systems Using Digital Twin Framework	1
<i>George Flutur, Ovidiu-Petru Stan, Gabriel Chindris, Liviu-Cristian Miclea</i>	
An Analysis of Time-Domain Period Jitter due to Random Telegraph Noise in Phase-Locked Loops	5
<i>Caroline P. Garcia, Gilson I. Wirth</i>	
Assessing the Limitations of Activation Clipping for Fault Mitigation in Vision and Language Transformers	11
<i>Lucas Roquet, Fernando Fernandes dos Santos, Luigi Carro, Angeliki Kritikakou</i>	
Automatic Enhancement of Cell Models to Enable Conditional Stuck-at Fault Simulation and Pattern Generation	17
<i>Reza Khoshzaban, Nikolaos I. Deligiannis, Iacopo Guglielminetti, Michelangelo Grosso, Riccardo Cantoro</i>	
Case Study: A Robust Bootloader System with Support for Over-the-Air Firmware Updates in CubeSat Payloads	23
<i>João Sobreira, Wendell Silva, Cícero Oliveira, Marcus Bezerra, Jarbas Silveira</i>	
Case Study: Exploring nMR Implementations for Energy Monitoring in Telecom Base Stations Under Non-Ionizing Radiation	25
<i>Elián Nevado, Jimmy Tarrillo</i>	
Case Study: Improving the Robustness of Photonic Neural Networks Against Memory Faults	27
<i>Mauricio Gomes de Queiroz, Leonardo Alexandrino de Melo, Mateus Vidaletti Costa, Salvatore Pappalardo Fabio Pavanella, Ian O'Connor, Alberto Bosio</i>	
Case Study: Integrating RISC-V Zicfiss Shadow Stack Support for Control-Flow Integrity on the CVA6 Processor	29
<i>Behnam Farnaghinejad, Ernesto Sanchez</i>	
Case Study: Neutron-Induced SEE Evaluation in a Mixed-Signal Programmable SoC	31
<i>Eduardo Lazzarotto Fabbris, Rafael Galhardo Vaz, Odair Lélis Gonçalves, Tiago R. Balen</i>	
Case Study: RISC-V Cores for Resource-Constrained Computing Systems Facing Neutrons	33
<i>P.-A. Peyronnet, L. H. Laurini, E. Atukpor, J. Guilbot, C. Costa, R. Possamai Bastos</i>	
Case Study: The High-Level Synthesis-Based Firmware Upgrade for the Digital Trigger Back-End System of the ATLAS Liquid Argon Calorimeter	35
<i>Melissa S. Aguiar, Dabson F. dos Santos, Adriana Milic, Diogo A. Cardinot, Marcos V. S. Oliveira Luciano M. A. Filho, Gustavo B. Libotte, Bernardo S. Peralva</i>	
Characterization of a Fault-Tolerant RISC-V SoC in an SRAM-based FPGA Under Proton Irradiation	37
<i>Wesley Grignani, Douglas A. Santos, Carolina Imianosky, Douglas R. Melo, Frédéric Wrobel, Luigi Dilillo</i>	
Convolutional Neural Networks for Energy Estimation in High-Energy Calorimetry	43
<i>Diogo Alves Cardinot, Bernardo Sotto-Maior Peralva, Gustavo Barbosa Libotte Luciano de Manhães Andrade Filho</i>	
Deep Learning-Based Power Side-Channel Evaluation from RTL Switching-Activity Proxies	49
<i>Behnam Farnaghinejad, Annachiara Ruospo, Alessandro Savino, Stefano Di Carlo, Ernesto Sanchez</i>	

Design and Reliability Analysis of a Pipeline RISC-V Processor Core	55
<i>Douglas A. Santos, Wesley Grignani, Carolina Imianosky, Douglas R. Melo, Luigi Dilillo</i>	
Design of a Low-Power High-Density Analog in-Memory Computing Accelerator Using 18 Nm FD-SOI Phase-Change Memory	61
<i>V. Viollet, G. Prenat, A. Al Muklash, C. Popon, L. Anghel, X. Lecoq</i>	
Embedded Tutorial: Design for EMC and Trust in Integrated Systems – Combining Robustness, Innocuity and Security Concerns	67
<i>Régis Leveugle</i>	
Embedded Tutorial: Security in Reconfigurable Scan Networks	69
<i>Joel Åhlund, Markus Törmänen, Erik Larsson</i>	
Emulating SDC-1 Hardware Faults Through Application Level Bit-Flip Injections in QNNs	73
<i>Giacomo Perlo, Antonio Porsia, Annachiara Ruospo, Ernesto Sanchez</i>	
Enhancing Fault Tolerance in Microblaze V Soft-Core Processors: Performance and Reliability Assessment with ESA Benchmark Applications	79
<i>Gabriel Camargo, Fabio Benevenuti, José Rodrigo Azambuja, Antonio Carlos Beck, Fernanda Kastensmidt</i>	
Enhancing the Lifetime of STT-MRAM in IoT Applications by Current Balancing	85
<i>Somayeh Sadeghi-Kohan, Fatemeh Akbari, Mahta Mayahinia, Mehdi B. Tahoori, Sybille Hellebrand Hans-Joachim Wunderlich</i>	
Evaluating an Analog Test Pattern Generation Tool by Means of Hardware-Emulated Fault Injection	89
<i>Luis A. Duarte, Lucas B. Zilch, Állan F. G. Ferreira, Marcelo S. Lubaszewski, Tiago R. Balen</i>	
Fast Statistical Estimation of Circuit-Level Cross Section Considering Logical Masking Effects	93
<i>Clayton R. Farias, Tiago R. Balen, Paulo F. Butzen</i>	
Fault-Tolerance in FINN-Based CNN Accelerator for In-Orbit Land Cover Classification	99
<i>Fabio Benevenuti, Ulisses Maffazioli, Arthur F. Ely, Eduardo Marañon, Antonio Carlos S. Beck José Rodrigo Azambuja, Fernanda L. Kastensmidt</i>	
Impact of Alpha-Induced Single Events on the Inference Confidence of Quantized Neural Networks on Cortex-M	105
<i>Leonardo R. Gobatto, Nathan Guimarães, Fabio Benevenuti, Antonio Carlos S. Beck Fernanda L. Kastensmidt, Jose Rodrigo Azambuja</i>	
LA-SCG: Layout-Aware Scan Chain Grouping for Peak Shift Power and IR-Drop Mitigation in Scan-Based Testing	111
<i>Rohit Badjatya, Harsh Gupta, Makoto Ikeda, Masahiro Fujita, Virendra Singh</i>	
LPCG: A Capture Activity-Aware Technique for Low-Power Scan Testing	117
<i>Rohit Badjatya, Jaydev Bapat, Makoto Ikeda, Masahiro Fujita, Virendra Singh</i>	
M-EL2N: Data-Efficient Fault Injection Through Sample Difficulty Analysis	123
<i>Nicolò Bellarmino, Alberto Bosio, Ahmed Al-Kaf, Mounir Benabdenbi, Régis Leveugle, Riccardo Cantoro</i>	
Mitigation of SETs Under Process Variability Effects: Circuit-Level Strategies for Reliable Design	129
<i>Marina L. Dias, Bernardo B. Sandoval, Paulo F. Butzen, Ricardo A. L. Reis, Cristina Meinhardt</i>	

PowerCourt: Formally Judging Benign-Looking Circuits in Multi-Tenant FPGA Environments	135
<i>Philipp Schmitz, Mohamed Shelkamy Ali, Dino Mehmedagić, Hassan Nassar, Jörg Henkel, Dominik Stoffel Wolfgang Kunz</i>	
Radiation Robustness Assessment of StrongARM Comparators in 130nm, 65nm and 45nm Technologies	141
<i>Bianca Nunes Coelho, Thales Stedile-Ribeiro, Tiago Roberto Balen</i>	
Resilience Analysis of a Fault-Tolerant MPSoC Interconnection Architecture Under SEU Fault Injection	145
<i>Thiago H. Rausch, Wesley Grignani, Luigi Dilillo, Douglas R. Melo</i>	
RESQ: A Unified Framework for ReLiability- and SEcurity Enhancement of Quantized Deep Neural Networks	151
<i>Ali Soltan Mohammadi, Samira Nazari, Ali Azarpeyvand, Mahdi Taheri, Milos Krstic, Michael Hübner Christian Herglotz, Tara Ghasempouri</i>	
Soft Error Mitigation in a Real-Time Control System Through Hardware Protection on an SRAM-Based FPGA	155
<i>A. Giuffra, J. Minaya, J. Tarrillo</i>	
Software Diversity in Resource-Constrained Embedded Systems	159
<i>Kush Dave, Ian G. Harris</i>	
Spectral Vs. Spatial Pruning: Fault Resilience Analysis for Extremely Sparse DNNs	163
<i>Manar Gani, Leonardo Alexandrino de Melo, Alberto Bosio, Rodrigo Possamai Bastos, David Novo</i>	
Susceptibility Evaluation of Layout-Based 2:1 Multiplexer Topologies	169
<i>Ana Flávia D. Reis, Eduardo A. C. da Costa, Rafael B. Schvitz</i>	
Towards Reliable and Scalable Firmware Testing in Communication-Constrained Environments	175
<i>J. D. S. Coutinho Filho, A. H. P. Dantas, T. D. de Araújo, J. E. Silva Filho, J. A. N. da Silveira A. A. M. de Albuquerque</i>	
Validating Statistical Delay Test Generation Under Timing Variations via SAT-Based ATPG	179
<i>Hanieh Jafarzadeh, Jan Dennis Reimer, Hussam Amrouch, Sybille Hellebrand, Hans-Joachim Wunderlich</i>	
Case Study: A Uniform Benchmarking of RISC-V Cores on FPGA — Performance, Power, and Area Analysis	185
<i>João Carlos Britto Filho, Paulo Francisco Butzen</i>	
Reliability Assessment of Deep Neural Networks and Accelerators Across Design Stages	187
<i>Mohammad Hasan Ahmadilivani, Natalia Cherezova, Michael Glaß, Juan-David Guerrero-Balaguera Maksim Jenihhin, Angeliki Kritikakou, Robert Limas Sierra, Leticia Bolzani Poelhs, Jaan Raik Lucas Roquet, Fernando Fernandes dos Santos, Felipe Augusto da Silva, Matteo Sonza Reorda Alessandro Veronesi, Ernesto Cristopher Villegas Castillo, Josie E. Rodriguez Condia</i>	