



The Adaptation of Industry-Grade Electronic Design Automation in VLSI Design Curriculum among Malaysia's Universities

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ABSTRACT

BACKGROUND & CONTEXT

As the semiconductor talent gap persists, engineers skilled in digital VLSI design are increasingly needed to support AI-driven industry advancement. Most engineering institutions rely on non-commercial EDA tools for VLSI courses, which are accessible and cost-effective but do not replicate the practical experience of industry-standard tools. At Universiti Teknologi Malaysia, third-year Electronics System Design and Microelectronics students undertake Basic Digital VLSI Design (SKEL 4743), covering MOSFET theory, CMOS technology, and circuit and logic design. However, the course previously lacked a clearly defined instructional method and a means of assessing its learning effectiveness.

PURPOSE OR GOAL

This study examines the use of blended learning combined with project-based learning (PBL), integrating industry-grade Mentor Graphics EDA tools, as the instructional approach for the course. It aims to assess whether this approach improves students' practical design skills and learning outcomes compared to prior cohorts.

APPROACH OR METHODOLOGY

Students completed a schematic-driven layout design project structured around two milestones: schematic design (Milestone 1) and physical layout using SDL techniques (Milestone 2), each assessed via technical and output visualization rubrics. A comparative analysis of course learning outcomes (CLOs) from the 2022/2023 and 2023/2024 sessions was conducted, supplemented by end-of-course reflection surveys.

OUTCOMES

CLO3/PLO5, which measures circuit and layout design ability, improved from 0.84 to 0.91 between the two sessions, while CLO2 (theory-based) declined, reflecting a shift toward stronger practical competency rather than reduced learning. Student satisfaction rose from 70% to 83%, alongside gains in perceived design skills and EDA tool adaptability.

CONCLUSIONS

The blended learning framework with industry-grade EDA tools effectively improved students' hands-on VLSI design capability, supporting existing evidence that integrating industry-relevant tools into project-based curricula enhances engagement and prepares students for real-world semiconductor design careers.

KEYWORDS

Project assignment, EDA tools, Milestone assessment.

Introduction

Digital systems are now highly demanding in nowadays life, with integrated circuit (IC) design complexity increasing from thousands to over a billion transistors. This growth enables more functionalities to be integrated into single IC chips. As integrated circuit technology rapidly advances, there is a critical need for innovation in the content and teaching methodologies of Very Large-Scale Integrated Circuit (VLSI) courses, as reported by Singh, A. K. (2023) and Kang, S.M. (2015). As the technology landscape rapidly evolves, driven by Industry 4.0 and the rise of artificial intelligence (AI), there is a pressing need for a new generation of engineers skilled in digital Very Large-Scale Integration (VLSI) design. Research by Al-Maadeed et al. (2020) and Li et.al (2022) highlights this demand, emphasizing that these engineers will be pivotal in creating the next wave of intelligent systems, from autonomous vehicles to advanced medical devices, all reliant on sophisticated integrated circuits.

To meet industry talent requirements, it is essential to incorporate design automation applications into university-level VLSI curricula, as strongly mentioned by Johnson, P. R., & Lee, S. (2019). This integration should include practical experiments, visual presentations of semiconductor device structures and processes, VLSI design flows, and the use of industry-standard simulation tools alongside advanced technologies as outlined by Lee, W. F. (2019). The aim is to cultivate students' innovative thinking and enhance their practical skills, addressing the urgent need to develop talent at universities to support the current and future landscape of IC design worldwide. Most engineering institutions use educational and non-commercial electronic design automation (EDA) tools for their VLSI design course. The main reasons include that non-commercial tools are more readily available, have a user-friendly interface, and are relatively cost-effective. Some of these tools may provide a decent introductory insight into IC design flow as claimed by Singh et.al (2023). However, non-commercial EDA tools usually cannot offer the practical experience with tools that the students will utilize in the real industry world.

To address this challenge, a project-based learning experience has been specifically designed for third-year Electronics System Design and Microelectronics students at Universiti Teknologi Malaysia. Basic Digital VLSI Design (SKEL 4743) is an undergraduate core course for third-year students pursuing a Bachelor's Degree in Electronics Engineering. The students must complete several prerequisite modules, including basic electronics and digital system design, where they gain foundational knowledge in electronics and introductory digital electronics, before admission to this course. The course material for SKEL 4743 covered everything from Metal Oxide Semiconductor Transistor (MOSFET) theory and Complementary Metal Oxide semiconductor (CMOS) process technology through circuit and logic design. Students have also learnt how to analyze logic circuit for process, voltage, and temperature (PVT) variations. This approach centers on hands-on projects that emphasize custom schematic-driven layouts, allowing students to explore the design of digital circuits, such as logic gates, Boolean algebra, and circuit implementation. By translating abstract concepts into functional circuits, students embark on a journey of discovery, constructing circuits from the ground up that follow the findings by Reddy, S. M. (2005). This process not only deepens their understanding of digital design principles but also encourages them to apply theoretical knowledge in practical scenarios, pushing the boundaries of their learning. In addition, all Malaysian universities offering Electronic Engineering programs are equipped with IC design EDA tools under an initiative by the Ministry of Higher Education (MOHE) in collaboration with the Academy of Semiconductor Malaysia. Therefore, there is no issue of infrastructure limitations, as standardized access has been provided nationwide.

This course prepares students for advanced VLSI design courses and equips them with the skills necessary to thrive in the competitive field, which supports the findings provided by Isaak, S. (2020). The students will emphasize ethical design considerations, encouraging students to think about the broader impact of their work and ensure their designs meet needs while respecting public health, safety, and the environment. This approach directly contributes to the

program learning outcome of designing solutions for complex engineering problems while considering ethical and societal implications.

This paper specifically examines the use of blended learning, combined with project-based learning (PBL), as the primary instructional approach for the Basic Digital VLSI Design course (SKEL 4743) offered to third-year Electronics System Design and Microelectronics students at Universiti Teknologi Malaysia. The blended learning model integrates online instructional content and in-person lab sessions, while the PBL component emphasizes hands-on, schematic-driven layout projects using industry-relevant tools. This pedagogical strategy enables students to apply theoretical knowledge to practical circuit design tasks, thereby deepening their understanding and enhancing skill acquisition. However, the original proposal did not clearly describe this instructional method, nor did it explain how the effectiveness of learning would be analyzed. To address this, the current study uses a comparative analysis of course learning outcomes achieved by students from the academic year 2023/2024 versus those from 2022/2023, serving as a method to assess the impact of the blended PBL approach on student performance. This assessment provides empirical support for refining VLSI education in response to rapid technological advancements and industry demands. The qualitative findings will be based on students' performance and measures of the following outcomes:

- i. CLO1/PLO1: Describe the integrated circuit technology and design process (measured through understanding and application).
- ii. CLO2/PLO3: Analyze logic circuits using MOS transistors (evaluated through problem-solving and analysis skills).
- iii. CLO3/PLO5: Design circuits and draw VLSI layout using CAD software (assessed through practical design and layout execution).

The paper is organized as follows: Section 2 covers the methodology of the VLSI design course. Section 3 presents the results and discussion on the findings of the utilization of industry-grade EDA tools. Finally, Section 4 concludes the paper.

Methodology

The project-based learning approach guides students through the entire design flow, from schematic capture to simulation, verification, and layout. They gain proficiency in using industry-standard Mentor Graphics EDA tools, gaining valuable experience with software used in real-world VLSI design environments. This hands-on experience prepares them for the complexities of advanced VLSI design courses and equips them with the skills needed to thrive in the competitive field of I.C design, as strongly suggested by Williams, A. R., & Xie, Y. (2021). The hands-on experience involves exploring logic gates, Boolean algebra, and circuit implementation. However, the project presents challenges in balancing complex design considerations and mastering industry-standard EDA tools. To support them in navigating these complex tasks, a milestone achievement framework has been implemented to support them in navigating these complex tasks. This framework is assisted with a blended learning approach, ensuring students effectively navigate the project completion using industry-standard EDA tools. Learning outcomes are assessed through milestone achievement and evaluated using technical and output visualization rubrics. This implementation is adapted the success framework found by Li, Y., Li, J., Zhou, Y. (2022).

The students can independently discover new industry-related skills, and the knowledge in the VLSI domain will be beneficial for future employment. The main objectives of this project-based learning approach are as follows:

- i. To validate students' competencies on analysing the combinational logic circuit.
- ii. To develop students' capability to design a full custom circuit using Mentor Graphics EDA tools, including the VLSI schematic and layout design.
- iii. To foster the task distribution commitment and completion in terms of teamworking.

The project-based learning session is conducted only seven weeks after mid-semester break. At this time, students have gained knowledge on CMOS combinational logic design theory and analysis. Therefore, it would help them to go through the project design and verification process. Figure 1 shows the framework used to visualize the flow of associating the blended learning method with project-based learning. In general, the project-based learning started with the design planning, followed by the methods used for delivery the learning and lastly the assessment. There are 6 hours of online tutorials and a practical, guided hands-on session with lecturers to support students in completing the project. Each team of three or four students is provided one week to develop a design proposal based on a given complex boolean equation, including a truth table and a stick diagram. Students attend short online meetings with lecturers to receive feedback and approval on their pre-circuit design based on a provided schedule. Upon approval, students can begin implementing the schematic and layout of the circuit using Siemens Mentor Graphics EDA tools, which the schematic and layout implementation also already examined by Lee, W. F. (2019) and Isaak, S., et. al (2020). These tools are easily accessible via the *AnyDesk* platform from student hostels or any location with internet access. Lecturers also provide tutorial videos on implementing circuit design using the dedicated EDA tool for this project. Assessment of this course includes assessments for the report, and short presentation, and a demo video.

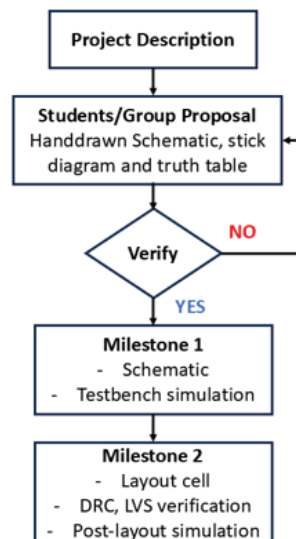


Figure 1: Framework of project-based assignments implementation

Guided Learning Phase

The pre-design phase sets the stage for the project-based learning experience, laying the groundwork for students to embark on their VLSI design journey. This phase involves a combination of theoretical instruction and practical application, preparing students for the challenges ahead. Lecturers provide a comprehensive briefing on the project, outlining the specific requirements, design goals, and performance targets. This includes defining the target technology, desired functionality, and any constraints on power consumption, area, or performance. Students are introduced to the industry-standard EDA tools, which include hands-on demonstrations and tutorials on the specific features and functionalities of Siemens Mentor Graphics, ensuring they are comfortable navigating the software environment. To foster a deeper understanding of the underlying design principles, students are guided through hand calculations for key design parameters to calculate the layout fill factor, estimate delay, and analyze power management strategies. These exercises help students grasp the theoretical concepts that underpin the design process. Each group of students is assigned a unique and complex Boolean expression. This serves as the foundation for their design,

requiring them to analyze the expression, understand its logic, and translate it into a functional circuit. Students create stick diagrams to visualize the layout of their circuit before embarking on the actual schematic design. This step allows them to explore different layout options, optimize the placement of components, and estimate the overall size and complexity of the final design. Students construct a truth table that accurately reflects the functionality of their circuit design. This serves as a crucial verification step, ensuring that their design meets the specified logic requirements. The truth table also allows them to predict the output behavior of the circuit for different input combinations, which can be further validated through pre- and post-layout simulations. Students schedule short online meetings with their lecturers to present their design proposals and receive feedback. This allows for early identification of potential issues, clarification of design choices, and guidance on optimizing the design before moving into the implementation phase.

Full Custom and Standard-Cell Design Methods

In this study, we implemented project-based learning focusing on two distinct design flows: custom design and digital design. For the digital design flow and custom flow, a systematic process is outlined in Figure 2.

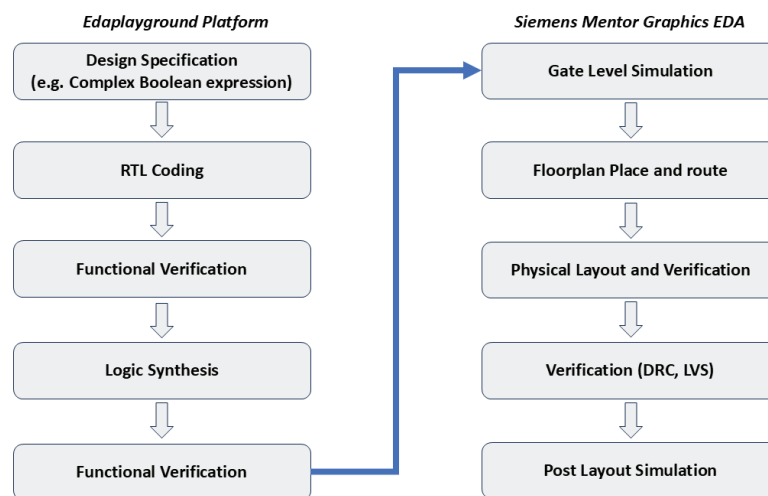


Figure 2: The digital design flow

The process begins with defining the project requirements and specifications, ensuring clarity on the desired functionality and performance metrics. Students then translate the specifications into Register Transfer Level (RTL) code, which serves as a high-level description of the design. This step involves verifying the correctness of the RTL code through simulation, ensuring that the design behaves as intended. Then, the verified RTL code is synthesized into a gate-level representation, optimizing for area, speed, and power. After synthesis, the gate-level design is simulated to confirm that it maintains the expected functionality. A floor plan is created to define the physical layout of the circuit, considering factors such as component placement and routing channels. The components are placed within the defined floor plan, and the routing of interconnections is established to create the complete design. This step involves generating the physical layout of the design, preparing it for fabrication. After that, the physical layout is verified to ensure it meets design rules and specifications. Finally, a post-layout simulation is conducted to validate the performance of the design after all physical considerations have been accounted for.

To ensure a comprehensive learning experience, student learning outcomes are assessed through a series of milestones: Milestone 1 and Milestone 2. These milestones incorporate

relevant technical and output visualization rubrics, providing a structured framework for evaluating progress and ensuring mastery of key concepts.

Milestone 1 – Schematic Module

Digital design flow was used and implemented using hardware description language (HDL). The main goal of this assignment is to design a combinational logic circuit using complementary CMOS based on the Boolean expression, for example $Z = \overline{abc}d + e + \overline{y}$ where $y = abc$. A Verilog file is generated using the named design.sv through EDA playground. The Verilog file is coded based on the Boolean function as shown in Figure 3.

```

design.sv
1 // Code your design here
2 module MKEL1163_ASSIGNMENT_1(a,b,c,d,e,z);
3   input a,b,c,d,e;
4   output z;
5   wire y;
6
7   assign y = ~(a&b&c);
8   assign z = ~(a&b&c&d) | e | ~y;
9
10  endmodule

```

Figure 3: RTL Verilog Code implemented in EDA playground

In this project, students utilized *LeonardoSpectrum* software to synthesize their RTL Verilog code design based on the given Boolean expression. This software supports Verilog source files and generates an optimized output file. The logic synthesis flow using *LeonardoSpectrum* follows these steps: First, students imported the Verilog design file into the software for synthesis. Next, they specified the target output directory and included timing constraints to aid in optimizing the design during the synthesis process. They then selected the target technology, specifically choosing “GDK_TSMC_013_type,” as illustrated in Figure 4. Finally, students synthesized the Verilog design file by clicking “Run Flow,” and created the netlist. Next, students imported the netlist file into the Pyxis Project Manager to generate a schematic from an existing symbol. Similar to the process in Leonardo, they map a library named sil013_kit for 0.13µm CMOS technology. Once completed, Pyxis Schematic converts the netlist file into a gate-level schematic. Then the students were required to perform the simulations to verify their design functionality and behaviours. The students performed a series of simulations to analyze the circuit's performance characteristics, including functional simulation to verify logic against the truth table, timing simulation to assess propagation delays and signal transitions, and power simulation to evaluate power consumption.

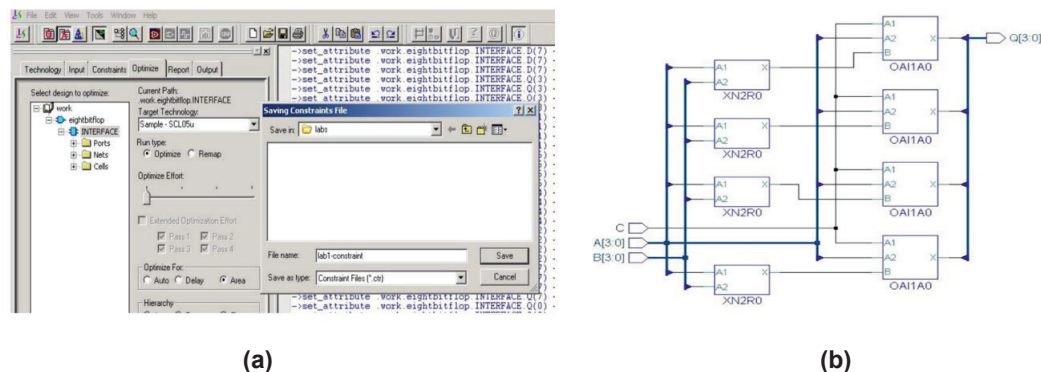


Figure 4: (a) Synthesize the design in Leonardo

(b) RTL schematic in Pyxis

Finally, students reported their design process and simulation results in a technical report, including a clear schematic diagram, a detailed description of the testbench, and a comprehensive analysis of simulation data. This report also includes a comparison of simulation results with the truth table, highlighting any discrepancies or unexpected behaviour, and a discussion of the circuit's performance characteristics and potential areas for improvement. Successful completion of Milestone 1 demonstrates the students' ability to translate their design concept into a functional schematic, test its behavior, and analyze its performance, laying the foundation for Milestone 2.

Milestone 2: Physical Layout and Verification

In Milestone 2, students transformed the schematic created in Milestone 1 into a physical layout using schematic-driven layout (SDL) techniques as shown in Figure 5. They utilize an EDA tool to place and route components, such as transistors and gates, according to the schematic while carefully adhering to design rules and layout constraints. To ensure compliance with these rules, they perform Design Rule Checks (DRC) and Electrical Rule Checks (ERC), identifying and correcting any violations. Additionally, Layout vs. Schematic (LVS) verification is conducted to confirm that the layout accurately reflects the schematic design. RC extraction is performed to create a SPICE netlist, which includes all components along with their resistance and capacitance values, known as the post-layout netlist. Following this, post-layout simulations are conducted before the tape-out process. Upon completion, the GDSII file format for the physical layout is generated and sent to the fabrication center. In the context of project-based learning, students complete their projects up to the GDSII creation stage.

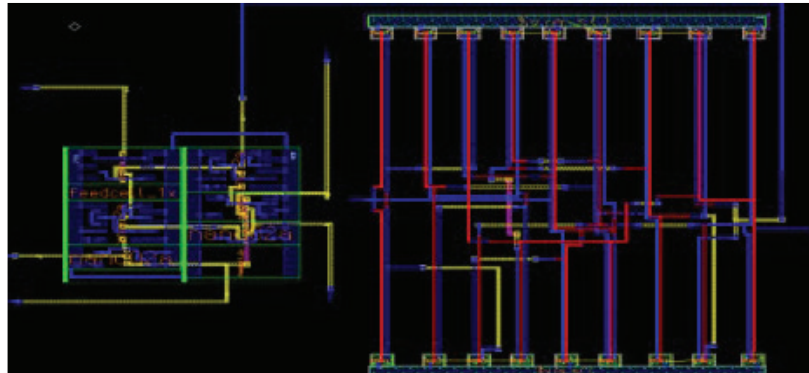


Figure 5: Layout of logic gate and sequential logic cell

Evaluation and Analysis

To scientifically evaluate the effects of the course reform, the project employed both quantitative and qualitative methods across several dimensions, including student knowledge acquisition, engineering skill development, attitude changes, and innovation capacity improvement. These evaluations focused on applied problem-solving, requiring students not only to understand theoretical concepts but also to apply them in practical circuit design. Moreover, students demonstrated enhanced engineering and technical competencies through the Mentor Graphics EDA tool usage.

- i. **Design Requirements:** Clarity in defining design specifications.
- ii. **Systematic Design Approach:** Effectiveness of the structured methodology for creating logic circuits and full custom layouts.
- iii. **Result Presentation:** Accuracy and clarity in displaying results using graphs, tables, and figures, with proper labeling.
- iv. **Data Verification:** Thoroughness in verifying data and highlighting significant findings.
- v. **Reporting and Presentation:** Quality of report writing and presentation, ensuring clarity and conciseness without ambiguity.

Evaluations of project reports and hands-on performance showed that students developed stronger independent thinking and could independently adjust and optimize circuit parameters, reflecting real progress in engineering capabilities. Surveys and interviews conducted after the course demonstrated that most students approved of the reformed content and methodology. They found the curriculum both challenging and engaging, especially valuing the industry-grade EDA tools usage. Many students reported that hands-on use of Mentor Graphics EDA helped them better understand the principles and applications of VLSI.

Learning Outcome Assessment

This study presents a blended learning framework for a project-based VLSI circuit design assignment that effectively addresses challenges associated with using industry-standard tools. Focused on a complex full-custom design employing Silterra 130 nm CMOS technology and Mentor Graphics, students demonstrated high achievement across various learning outcomes over two academic sessions, and the introduction of industry-grade EDA tools significantly improved key performance indicators in subsequent years as depicted in Table 1. Evaluated through a comprehensive rubric, this approach enhanced student engagement and learning outcomes, highlighting the effectiveness of integrating industry-grade tools with face-to-face learning in preparing students for the future in I.C design. This study focuses on CLO3/PLO5, emphasizing students' ability to design circuits and VLSI layouts using CAD tools. Although CLO2 scores declined, it assesses exam-based theory, not practical skills. Improvement in CLO3 indicates enhanced hands-on capability, showing CLO2's decrease does not impact CLO3's implementation or intended learning outcomes.

Table 1: Course Learning Outcome and Program Learning

Outcome CLO/PLO achievements		
CLO/PLO	2022/2023	2023/2024
1	0.68	0.7
2	0.77	0.66
3	0.84	0.91

Surveys Analysis

Students' perspectives on their learning experience were assessed through reflection surveys after project assignments. Table 2 summarizes responses to five qualitative questions from the second semesters of the 2022/2023 and 2023/2024 academic sessions. Many students expressed enthusiasm for designing complex digital VLSI with Mentor Graphics, enhancing skills transferable to the industry. Issues included teamwork difficulties, dissatisfaction with teammates' responsibilities, and limited skills in MOS transistors. Despite this, 83% of students reported satisfaction with the process in 2023/2024, up from 70% in 2022/2023. Improved virtual machine setups also supported better performance.

Table 2: Responses of end-of-course survey

Remark	2022/2023			2023/2024		
%	Agree	Neutral	Disagree	Agree	Neutral	Disagree
Enhanced design skills	70	25	5	83	17	0
Time durations	60	20	20	77	23	0
Teamwork commitment	68	15	17	72	17	11

Visualize career/job in semiconductor	74	26	0	85	15	0
Adaptability of EDA tool	67	26	7	79	14	7

Conclusions

This paper demonstrated that the students also have the opportunity to implement the project assignment based on an industrial perspective, whereby they can tailor the learning experience in VLSI design according to industrial needs. The designed evaluation metrics give comprehensive results to overcome the problem based on students' reflection on how this course was conducted. The blended learning framework for VLSI circuit design proved effective in addressing challenges associated with industry-standard tools. The integration of virtual labs, face-to-face, and online learning consistently improved student performance, particularly in design circuits and drawing VLSI layout using EDA tools, demonstrating the value of hands-on experience with industry-grade tools like Mentor Graphics. The success of the project-based assignment approach can be attributed to careful syllabus planning, appropriate prerequisites, and the use of industry-standard IC design tools. This approach enabled students to learn both full-custom and standard cell design techniques and participate in a meaningful design project that required the application of both methodologies. The successful completion of complex designs further highlights the adaptability and effectiveness of incorporating industry-grade Mentor Graphics in this course. These findings suggest that blended learning frameworks can significantly enhance student engagement and learning outcomes in VLSI design, ultimately contributing to their success in the field of integrated circuit VLSI design.

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Acknowledgements

The authors acknowledge the generous support of Emerald Systems Sdn. Bhd., who provided insightful guidance through their Siemens Mentor Graphics manual and Silterra 130 nm CMOS Technology library. We are deeply grateful to our stakeholders, MIMOS-MIDA-EEPN-CREST, for their support through the National IC Design Talent 2019-2025 Program. We also extend our sincere thanks to the Faculty of Electrical Engineering, University Teknologi Malaysia, for providing the necessary laboratory workstations.

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